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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,926	09/13/2000	Nobuaki Tokushige	900-348	7467

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,926	TOKUSHIGE, NOBUAKI	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7-9,11 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-5, 7-9, 11 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 4-5, 7-9, 11 and 24, insofar as being supported by elected Species I along with Species II, are objected to because of the following informalities and/or defects:

Claims 1, 7 and 24 each recite the subject matter that at least one transistor is formed "on and in" a semiconductor layer, but a transistor cannot be fully on and in a semiconductor simultaneously. And, they each fail to clarify that only the channel portion and the source/drain portions of the transistor are formed in the semiconductor layer, while the electrodes are formed on the semiconductor layer.

Furthermore, claims 1 and 7 each recite the terms of "an impurity diffusion layer" (or, "a well"), and "a P-type well" (or, "a N-type well"), but fail to clarify what are their relationships.

Claims 4 and 8 each recite the limitation of "the bias voltages are applied to the well; while in claims 1 and 7, each defines that the bias voltages are not for "the well" alone, but also being applied to the (well of the) other of the two transistors.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 4-5, 7-9, 11 and 24, as being supported by the elected species, are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matters which were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Each of claims 1, 7 and 24 recites the subject matters that the active regions of the first and second transistors are substantially completely depleted simultaneously in the standby state. However, the original disclosure lacks an adequate description regarding how the two active regions of CMOS-type-paired transistors can be substantially completely depleted simultaneously at the standby state, given the fact that the standby state is still an operative state in which the individual gate thresholds have been increased/decreased, so that the leaking current can be reduced during the off state; and that when paired CMOS-type transistors are in an operative state, only one of the two transistors is in the off state, while the other one is in the on state, even through they may also in the standby state. It is not clear how the on-state transistor can also have a completely depleted active region. Applicant's relevant arguments filed on July 30, 2004, fail to point out where exactly in the original specification support for such recited subject matters can be found, especially the subject matter regarding the recited limitation of "simultaneously".

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4-5, 7-9, 11 and 24, as being supported by the elected species, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 7 and 24 each recite the subject matters that the recited two wells are substantially electrically isolated from each other, but the disclosure lacks an adequate definition regarding to what degree the recited two wells have to be electrically isolated from each other in order to meet the recited term of "substantially electrically isolated from each other". And, according to the elected species, the two wells are only separated from each other by a portion of the doped semiconductor substrate, and there still has a diode-type coupling between the two wells (see Fig. 4d), instead of being electrically isolated from each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-5, 7-9, 11 and 24, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections, are rejected under 35

U.S.C. 103(a) as being unpatentable over Burr (US 6,072,217) in view of Yamaguchi (US 5,557,231) and/or 96-12470 (" K'470"; Korean Patent Publication, of record).

Burr discloses a fully-depleted-type semiconductor device (see Figs. 4-6, 7 and 8), comprising: a first MOS transistor (with gate 518; n-type) with source and drain regions (512, 514) in a semiconductor layer formed on a semiconductor substrate (510; p-type); buried insulating film (508); a first back gate formed of a p-type well (540/544) in substrate (510); a second back gate formed of an N-type well (542/546) in the substrate underlying a second MOS transistor (with gate 526; p-type), wherein the two wells are substantially separated from each other.

Burr further teaches to tune the threshold voltages of the transistors to reduce the leakage current in their standby state (see col. 2, lines 4-8). Although Burr does not explicitly disclose that such tuning of threshold voltages involves applying different bias voltages to the two back gates in the active and standby states, such changes of bias voltages are well recognized as being essential in the art in order to achieve low leakage and low power consumption in the standby state and fast speed in the active state, as evidenced in the prior art such as Yamaguchi (see Figs. 16-18).

Although Burr does not expressly disclose that back gate structure can further comprise a contact portion of a contact region formed in a device isolation region that isolates it from the semiconductor layer, one of ordinary skill in the art would readily recognize that a back-gate contact portion can be readily formed in a device isolation region which isolates it from the semiconductor layer for forming the contact to the back gate with improved device isolation without wasting additional spaces, as evidenced in

K'470 (see the contact portion 31 formed in the device isolation region 16 which isolates it from the semiconductor layer (including 14) in Fig. (D)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the back-gate bias of Yamaguchi and the back-gate contact structure of K'470 into the semiconductor device of Burr, so that a semiconductor device with desired active/standby states and with improved device isolation without wasting additional spaces would be obtained.

Regarding claims 1, 4 and 5, it is noted that one of ordinary skill in the art would readily recognize that only a portion of the back gate well that is directly underlying the channel region can control the state of the channel region; and, that the back-gate diffusion well in the bottom substrate can be as wide as being also underlying the source/drain regions, so as to ease the patterning and alignment requirements, as further evidenced Burr (see the back gates 432, 434 in Fig. 4, and back gate 854 in Fig. 8) and/or in K'470 (see the well 24 which extends laterally beyond the edges of the source/drain regions).

Response to Arguments

4. Applicant's arguments filed on July 30, 2004, have been fully considered but they are not persuasive.

Applicant's main arguments include: (A). Burr teaches that the well regions cannon extend outside the S/D regions thus cannot receive the contact as claimed; and, (B). The back gate in K'470 is always the same conductivity type as the S/D regions.

In response, it is noted that Argument A indicates the subject matters that the recited contact is located between S/D regions of neighboring transistors so that the well regions have to extend beyond the edges of the S/D regions in order to receive the recited contact. However, such subject matters are not necessarily recited in the rejected claims, as the contact to the back gate can also be formed at other locations such as the one in Fig. 8(a) of the instant disclosure (see the contact location 50).

In addition, Burr does teach that the back gate can be extended below the S/D regions (see the back gates 432, 434 in Fig. 4, and the back gate 854 in Fig. 8).

With respect to Argument B, the back gate in K'470 is always the opposite conductivity type of the S/D regions, as K'470 expressly states that for a MOSFET of the first conductivity type (i.e., the conductivity type of the S/D regions) the back gate well is the second conductivity type (see the English abstract provided before by the applicant).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
November 10, 2004

SHOUXIANG HU
PRIMARY EXAMINER